



Short communication

Reactive Spray Deposition Technology – An one-step deposition technique for Solid Oxide Fuel Cell barrier layers

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ABSTRACT

In order to reduce the cost of the manufacturing of Solid Oxide Fuel Cells (SOFC), and to enable metal supported cell fabrication, a new fabrication method called Reactive Spray Deposition Technology (RSDT) for direct deposition of the material onto ceramic or metal support for low temperature SOFC is currently being developed. The present work describes the effect on the performance of a SOFC when a $Gd_{0.2}Ce_{0.8}O_{1.9}$ (GDC) layer has been introduced as diffusion barrier layer between the yttria stabilized zirconia (YSZ) electrolyte and the $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ (LSC) cathode. The dense, thin and fully crystalline GDC films were directly applied by RSDT, without any post-deposition heating or sintering step. The quality of the film and performance of the cell prepared by RSDT was compared to a GDC blocking layer deposited by screen printing (SP) and then sintered. The observed ohmic resistance of the ASC with a GDC layer deposited by RSDT is $0.24 \Omega \text{ cm}^2$, which is close to the expected theoretical value of $0.17 \Omega \text{ cm}^2$ for a 5- μm thick 8 mol% yttria YSZ (8YSZ) electrolyte at 873 K.

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1. Introduction

Fuel cell technology has enormous promise for efficient and environmentally friendly mobile and stationary power applications. The reduction of the operating temperature of SOFCs (773–923 K) is an effective approach for reducing the cost of applied materials and increasing the lifetime for SOFCs. Resistive losses in electrolyte and electrodes must be reduced to achieve higher power densities at lower temperatures. Highest resistive losses in state-of-the-art anode-supported SOFCs come from the lanthanum strontium manganese–yttria stabilized zirconia (LSM–YSZ) composite cathode and its interface with the YSZ electrolyte, especially in the SOFC intermediate temperature range 773–923 K [1]. Therefore, SOFC systems operating below 973 K require a better cathode materials.

Several investigators have reported high conductivity for mixed ionic and electronic conductors like $La_{1-x}Sr_xCo_yFe_{1-y}O_{3-\delta}$ (LSCF) at 773–973 K compared to LSM [2–10]. However, LSCF reacts with YSZ, resulting in the formation of insulating $SrZrO_3$ [3,10–12]. Rose et al. reported that GDC layers produced by spin coating can successfully prevent diffusion and give good electrochemical performance with an ohmic resistance RS of $0.46 \Omega \text{ cm}^2$ [13].

In this work, we have studied the application of GDC diffusion blocking layers for high performance low operating temperatures

SOFC. The dense GDC layer has been deposited through the RSDT, which is a flame-based process involving spraying and combustion of a solution containing precursors of the ceramic materials [14]. RSDT uses the solvent as fuel and the flame provides both the heat for decomposition and the transport medium for resulted vapours and/or nanoparticles. This gives an open atmosphere, direct deposition method for ceramic thin layers with high adhesion and no need for additional heat treatment. By tuning the process parameters, layer morphology can be changed from dense to porous. In order to avoid thermal shocks in the porous substrates the substrates are heated from the back to match the temperature of the deposition flame. The RSDT technique has the advantage of lower GDC layer densification temperature, which prevents the solid state reaction between the GDC-barrier layer and YSZ electrolyte. Moreover, production of each cell component involved different techniques, requiring separate processing and sintering steps [15,16]. This leads to potentially complex multi-step industrial processes. Therefore, RSDT can be considered as a good alternative for the expensive Physical Vapour Deposition (PVD) process for applying a thin and dense GDC-barrier layer onto the electrolyte. Excellent cell performance of prepared anode-supported cell with LSC cathode and GDC-barrier layer deposited by RSDT has been obtained at an operating temperature as low as 773 K, using H_2 as fuel.

2. Materials and methods

The anode supported electrolyte (ASE) support consisting of NiO, pore former and 3 mol% YSZ (3YSZ) was made by tape casting

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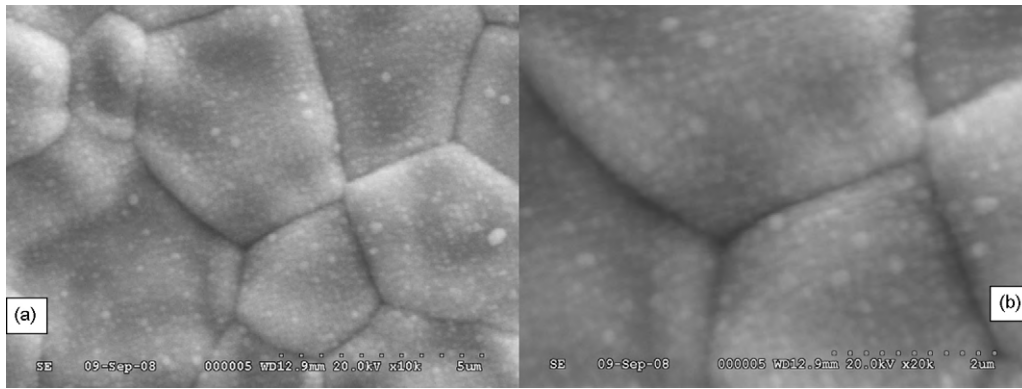


Fig. 1. SEM images of a GDC layer deposited by RDST on YSZ electrolyte; high magnification, top views of the coating: (a) $\times 10,000$, (b) $\times 20,000$.

and the resulting green tape was cut in $5\text{ cm} \times 5\text{ cm}$. Subsequently, the functional anode layer ($\text{NiO}/\text{Y}_{0.15}\text{Zr}_{0.85}\text{O}_{2-\delta}$, 8YSZ) and electrolyte layer (8YSZ) were applied by screen printing (SP) and co-fired at 1673 K for 1 h. The sintered anode electrolyte support consists of an approximately $550\text{ }\mu\text{m}$ thick anode substrate, an $8\text{ }\mu\text{m}$ thick electrochemical active anode functional layer and an $8\text{ }\mu\text{m}$ thick electrolyte layer. Two techniques have been used to prepare the GDC-barrier layers: SP and RDST. A toluene-based solution containing Ce and Gd alkoxides as precursors has been used as a precursor material for the layer prepared by RDST. During the deposition process the substrate temperature has been measured with a K-type thermocouple placed parallel and in contact with the substrate's surface. The substrate temperature during depositions was around 1223 K. GDC layers have been deposited on half cell substrates described above and Si wafer substrates using an RDST instrument similar to that described in [14]. Coating morphology and thickness have been investigated by SEM (Hitachi S-3500N) on both Si and half cell substrates. Elemental composition of the coating has been confirmed by EDXS using an Oxford X-ray spectrometer attached to the SEM. Phase composition has been analysed by XRD on a Brücker D8 Advance diffractometer (Cu cathode). Si supported coatings have been used for both chemical and phase analyses. The preparation details using the SP techniques have been described elsewhere [17]. The LSC cathode was screen-printed on top of the half cell with a 200 Mesh sieve and subsequently sintered at 1273 K for 1 h. The resulting cathode layer with dimensions of $32\text{ mm} \times 32\text{ mm}$ (electrochemical active area of 10 cm^2) has a thickness of ca. $35\text{ }\mu\text{m}$.

The cell performance was evaluated in a $5\text{ cm} \times 5\text{ cm}$ cell housing with corrugated ceramic flanges for good gas distribution. Platinum (Pt) meshes were used for current collection on both anode

and cathode sides. A weight of 2.5 kg was placed on top of the cell housing for a better contact between the current collector and the electrodes. The anode side was flushed with humidified hydrogen with a flow rate of 500 ml min^{-1} . On the cathode side, synthetic air (20% H_2 and 80% N_2) was supplied as oxidant with a flow rate of 400 ml min^{-1} and 1600 ml min^{-1} , respectively. The current density and voltage value were recorded as a function of operating temperatures in the range 873–1073 K. The impedance measurement has been performed for all tested cells at a current density of 0.4 A cm^{-2} , using a Solartron Schlumberger frequency response analyzer (FRA) model 1255 in conjunction with a Schlumberger Potentiostat model 1287A. The applied frequencies were in the range of 0.01 Hz to 1 MHz with signal amplitude of 10 mV. The obtained Nyquist plots were fitted using the ZView2 fitting program and the contribution of the ohmic and electrode resistance to the total cell losses has been determined.

3. Results and discussion

3.1. Morphology of the GDC film prepared by RDST

The GDC diffusion blocking layer coatings have been applied using RDST on $5\text{ cm} \times 5\text{ cm}$ ASE substrates provided by ECN. The temperature of the flame was constant at ca. 1223 K. The deposition rate was 2 ml min^{-1} but could be further increased for deposition on the bigger substrates. The coatings exhibit a dense, continuous and homogenous microstructure. The thickness of the GDC layer is ca. 450 nm . The coating is uniform, excepting the edges of the substrate, where a rather strong edge effect caused by the substrate holder can be observed. No loss of adherence to substrate has been

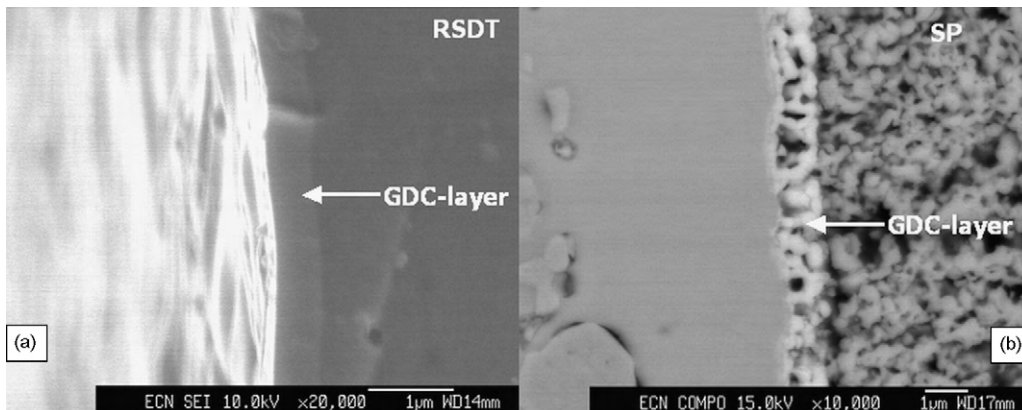


Fig. 2. Cross-sectional SEM images of GDC coatings deposited on YSZ electrolyte. (a) By RDST, (b) by SP.

Table 1
Elemental analysis of a 20% GDC ($\text{Gd}_{0.2}\text{Ce}_{0.8}\text{O}_{1.9}$) layer on Si wafer (as reported by the LinkISIS software, Oxford Instruments).

Element	Spectrum type	Intensity corr.	Std. corr.	Element (%)	Atomic (%)
Ce L	ED	1.100	0.99	72.50	74.74
Gd L	ED	1.036	0.99	27.50	25.26
Total				100.00	100.00

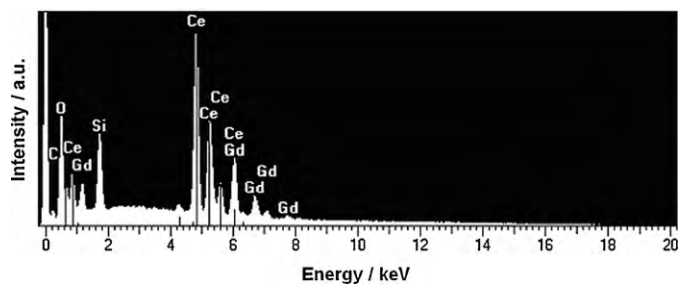


Fig. 3. EDXS spectrum of the RSDT-made GDC coating on a Si (2 0 0) wafer showing Ce L and M lines.

observed so far. The SEM images of a GDC coating on ECN substrate are shown in Fig. 1.

The coating is homogenous and very thin, so that the morphology of the underlying YSZ electrolyte layer is perfectly visible. At high magnification the fine morphology of the top layer of the coating becomes visible. It consists of homogeneously distributed 50–100 nm large growing centres (grain tops), as seen in Fig. 1b. Coverage seems good and uniform. Fractured cross-sections of the GDC/electrolyte assembly are shown in Fig. 2a and b. The coating is dense and homogenous, no difference can be observed over substrate's grain boundaries. The electrolyte/coating interface is continuous and the adherence is good (the area observed during the SEM investigation was much larger than compared to area shown in Fig. 2, typically a few centimetres. The typical thickness of the layer is 450 nm, as shown in Fig. 2b.

3.2. Elemental analysis

Compositional analysis has been carried out using EDXS. Samples with similar GDC coatings on Si wafer substrates have been used. The elemental composition, as reported by the EDXS software, is presented in Table 1. The fact that the measured composition indicate a Gd/Ce atomic ratio (ca. 0.25/0.75) slightly higher than the expected Gd/Ce ratio (0.2/0.8 at.%) is an EDXS artefact caused by the superposition of Ce Ly and Gd L α lines, as shown by the spectrum in Fig. 3.

Phase analysis by XRD has been carried on the same Si supported samples used for EDXS. A spectrum is shown in Fig. 4. Phase analysis by XRD shows pure polycrystalline GDC having sub-micron grains with parallel orientation (a combined result of substrate's own orientation – the wafer is a (2 0 0) cut – and of the vapour phase growth). It is important to notice that the fully crystalline state has been observed without any further sintering. If this technology were to be used to deposit all the SOFC layers there would be a significant cost saving on material and energy.

3.3. Cell performance

The implementation of the ceria barrier layer using RSDT in the anode-supported cell leads to improvement in cell performance, which is shown in Figs. 5 and 6. These figures illustrate the cell performance improvement in terms of IV-curves (Fig. 5) and area specific resistance values (ASR), which are subdivided in polarization and ohmic losses (Fig. 6). As can be seen, the electrochemical

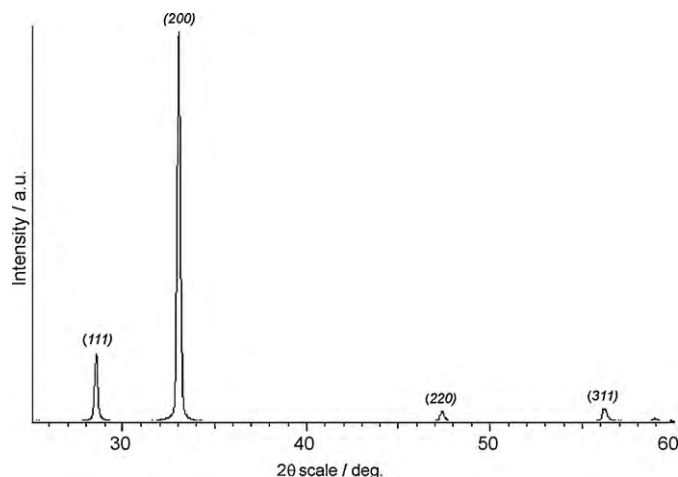


Fig. 4. XRD spectrum ($\text{Cu K}\alpha_1$) of GDC coating deposited by RDST on Si (2 0 0) wafer.

performance of anode-supported cell has been further enhanced by optimizing the quality of the ceria diffusion barrier in order to fulfill three requirements for the ceria layer. First, this layer has to be thin in order to reduce the ohmic contribution. Second, the ceria barrier layer has to be applied at temperatures as low as possible in order to prevent inter-diffusion of cations between the ceria and zirconia layers. This process creates an undesirable reaction zone with a lower ionic conductivity that results in enhanced ohmic losses [18,19]. Third, this layer must be dense in order to prevent any reaction between cathode and zirconia electrolyte [20]. The ceria layer preparation by means of RSDT is a suitable technique which meets those requirements. The GDC-layer prepared by RSDT technique is very thin (ca. 450 nm compared to 1.5 μm for the screen-printed one), which contributes to the reduced ohmic resistance. This technique has also the advantage of depositing crystalline GDC layer at temperatures that are lower than the usual sintering temperature of GDC, which avoids the undesirable reaction between the

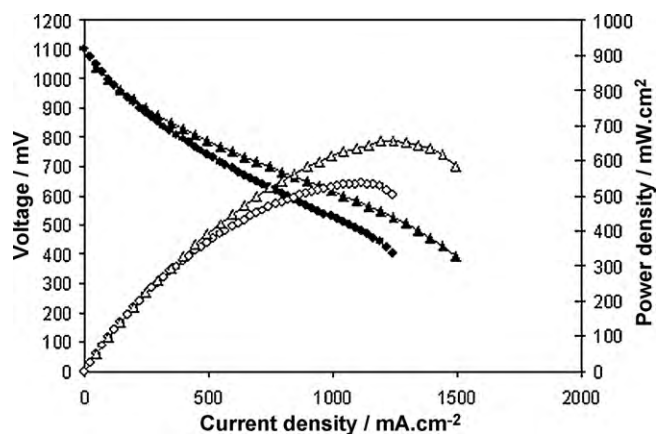


Fig. 5. Cell voltage and power density as function of current density at 873 K with humidified H_2 (500 ml min^{-1}) supplied to anode and synthetic air (400 ml min^{-1} O_2 and 1600 ml min^{-1} N_2) supplied to cathode; (\blacktriangle) ASC with RSDT-made GDC diffusion blocking layer; (\bullet) ASC with screen-printed GDC diffusion blocking layer.

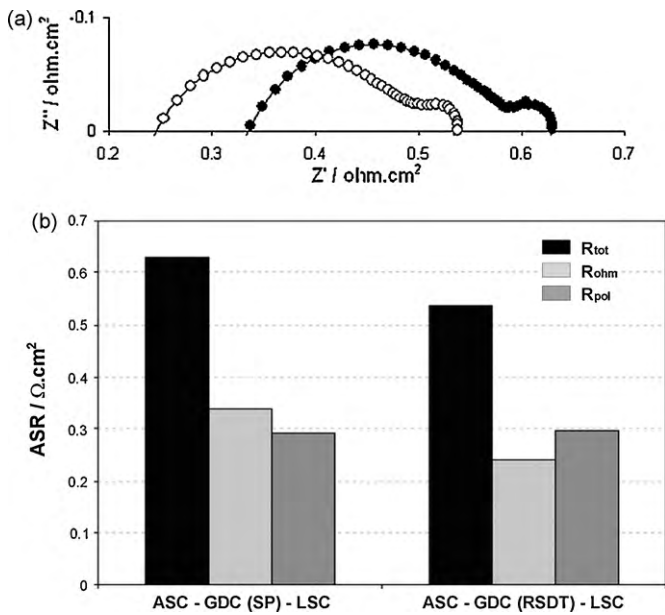


Fig. 6. (a) Nyquist plots for each cell configuration. (○) ASC with RSDT-made GDC diffusion blocking layer; (●) ASC with screen-printed GDC diffusion blocking layer. (b) Total area specific resistance (R_{tot}), ohmic losses (R_{ohm}), and electrode polarization losses (R_{pol}) for each cell configuration.

ceria layer and 8YSZ electrolyte. In addition, a higher contact area between the GDC and 8YSZ layers can be expected because of the better coverage of the substrate that a vapour based deposition method as RSDT offers compared to a powder based coating method as SP. As consequence, by applying the RSDT to deposit GDC-barrier layer onto the zirconia electrolyte, a peak power density of 656 mW cm^{-2} was obtained at an operating temperature of 873 K, as shown in Fig. 5. The main improvement is due to further diminished ohmic resistance values (Fig. 6). It can be attributed to the much thinner GDC layer made by RSDT and to its homogenous and dense nature, as shown by the SEM images in Figs. 1 and 2. This result supports the findings of Uhlenbruck et al. [21] who demonstrated that a good quality and dense GDC layer inhibits the formation of Sr–Zr oxides by diffusion of strontium from the cathode into the 8YSZ electrolyte, which further results in reduction of ohmic losses.

4. Conclusions

The present work shows that the RSDT technology has been successfully used as a one step manufacturing process to deposit a fully crystalline, thin and dense GDC diffusion barrier layer. A significant gain in cell performance has been obtained using H_2 as fuel and anode-supported cells with thin and dense film zirconia

electrolyte and RSDT-made diffusion barrier layer. The main gain in performance was due to a significant reduction in ohmic losses. The observed ohmic resistance of the ASC with GDC layer deposited by RSDT is $0.24 \Omega \text{ cm}^2$, which is close to the expected theoretical value of $0.17 \Omega \text{ cm}^2$ for a $5\text{-}\mu\text{m}$ thick 8YSZ electrolyte at 873 K. This indicates that the obtained peak power output density is approaching to what is theoretically possible. The RSDT technology has the potential to chain successive coating steps, significantly simplifying the production of multilayered ceramic structures as the SOFCs. A future study will be conducted to optimize the thickness of the GDC layer prepared by RSDT for a good balance between performance and durability as well as to better explain the effect of RSDT-made layers on the electrochemical activity of the cathode–electrolyte interface.

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